DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed March 10, 2008 have been fully considered but they are not persuasive.

2. Regarding claims 1 and 14, applicant argues "that neither the cited portions of Roberts, nor any other portion thereof, discloses or suggests at least the features of a plurality of reset signal lines disposed along the row direction, each being associated with one pixel row for supplying a reset signal" and requests that the Examiner point out specifically where this teaching is found in Roberts. In the previous non-final office action mailed on December 11, 2007, the Examiner specifically pointed out two sections of the specification in Roberts which teaches this limitation. Particularly, column 8, lines 44-55 and column 7, lines 11-26 were referenced in order to show that the sensor of Roberts includes reset signal lines. Specifically, the FET (68, 70) of Roberts is used to connect the capacitor (44) to the trace (54) in order to reset the pixel. As pointed out by the Examiner in column 8, lines 44-55, the traces 56 and 58 are used to send a logic signal to the FET (70) to connect the capacitor (44) to the trace 54 thereby resetting the pixel. Although, the Examiner should have specifically referenced traces 56 or 58 as the reset signal lines, the Examiner did specifically point out the sections of Roberts that teach this limitation. Furthermore, it is noted that the Examiner has referenced only the first embodiment of Roberts when the features of the second embodiment of Roberts were also referenced in the rejection. It is noted that the 2nd embodiment adds additional features to the 1st embodiment. See column 11, lines 50-68. As such, although they are given different reference

numbers (56 and 58 vs. 56' and 58'), the traces 56' and 58' are the same thing as in the 1st embodiment.

3. Additionally applicant argues that Roberts does not disclose "an overall reset controller for supplying an overall reset signal to all of said reset signal lines at one time" and requests that the Examiner point out specifically where this teaching is found in Roberts. In the previous non-final office action mailed on December 11, 2007, the Examiner specifically pointed out element 208 as being the overall reset controller and referenced column 12, line 28-50. Column 12, line 28-50 specifically states that pixels of the array all reset simultaneously. Furthermore, since the control cache (208) acts to buffer memory for pixel resetting (col. 13, lines 30-35), it acts as an overall reset controller.

4. Additionally, applicant argues that "Element 40' of Fig. 9 is not a switching circuit electrically connected to the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in the photoelectric converter element and discharge of the electric charge". However, the Examiner was broadly interpreting the entire pixel circuit (40') as being the switching circuit since it operates to control the generation of an output signal from the photoelectric converter element. If applicant continues to argue this, the are several switches (FETs) within the pixel circuit (40') which can be interpreted as being the claimed switching circuit. In particular any of FET's 46', 74', or 76' can be interpreted to be the claimed switching circuit since all of these switches operate to generate a output signal representing electric charge from the photoelectric converter element and all are electrically connected to the cathode of the photoelectric element.

5. Furthermore, applicant argues that the row selection and reset functions are performed in a row-by-row order. However, the Examiner's position in the previous office action mailed on December 11, 2007 was that this section pointed out shows that the rows are accessed in a sequential manner for reading and reset as claimed in the "row shift circuit" limitation. The section pointed out by the Examiner (col. 7, lines 10-47) does disclose that the rows are accessed sequentially. The main point of the section pointed out by the Examiner was that the saturation of the pixels which would occur in the conventional manner is obviated using a rolling shutter method. Clearly, as pointed out in col. 7, lines 10-47, the pixels are reset in a sequential row order using the rolling reset. Thus, it is the opinion of the Examiner that the sensor includes a row shift circuit (latch and decoder circuit, 24) that reads and resets sequentially using the rolling shutter. Additionally, it is the opinion of the Examiner that while Roberts does teach that the pixels are saturated using the conventional row-by-row technique, Roberts discloses a method of solving this problem, using the rolling shutter.

6. Furthermore, applicant argues "that the total recitation of the portion of claim 1 in question, i.e., "a row shift circuit including a row read scan circuit capable of supplying a read signal to said plurality of row selection signal lines sequentially, the rowshift circuit having no random access function" recites a row shift circuit having the specified structure and having no random access function and, therefore, is not a negative limitation." However, the Examiner maintains that the recitation of the limitation of the row shift circuit having no random access function is negative limitation. Thus, this rejection will be maintained.

7. For the reasons stated on the preceding pages, the rejections from the previous office action will be repeated.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 4-8, 10-13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts (U.S. Patent No. 5,452,004).

10. Regarding ***claim 1***, Roberts discloses a MOS-type solid-state image pickup device, comprising: a semiconductor substrate (Fig. 1, element 14); a large number of pixels arranged in one surface of the semiconductor substrate in an array having a plurality of rows and a plurality of columns (Fig. 1, element 12), each pixel (Fig. 1, element 40') including (a) a photoelectric converter element having a cathode (Fig. 9, element 42') and (b) a switching circuit (Fig. 9, element 40, broadly interpreted to be the entire pixel element, excluding the photodiode, since the entire pixel operates to output a signal representing electrical charge; it can also be more narrowly interpreted as being FET's 46', 74', or 76') electrically connected to the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in the photoelectric converter element and discharge of the electric charge (col. 8, line 44-55); a plurality of row selection signal lines (Fig. 2, element 56') disposed along a row direction, each being associated with one pixel row for supplying a row selection signal; a plurality of output signal lines (Fig. 9, CCVL) disposed along a column, each being associated with at least one pixel column; a plurality of reset signal lines (Fig. 2, element 58') disposed

along the row direction, each being associated with one pixel row for supplying a reset signal (col. 8, lines 44-55; col. 7, lines 11-26); a power source line (Fig. 2, element Vssa); and an overall reset controller (Fig. 1, element 208; col. 12, lines 28-50; since the control cache (208) acts to buffer memory for pixel resetting (col. 13, lines 30-35), it acts as an overall reset controller) supplying an overall reset signal to all of said reset signal lines at a time; wherein said switching circuit comprises: a series connection of an output transistor (Fig. 2, element 74) and a selection transistor (Fig. 2, element 76) connected between the power source line and an associated output signal line, the output transistor having a gate being capable of receiving a potential generated by the charge accumulated in said cathode (Fig. 2, element 72), the selection transistor having a gate connected to an associated row selection signal line (Fig. 2, element 80); and a reset transistor connected between said cathode and said power source line (Fig. 2, element 70); and having a gate connected to an associated reset signal line (Fig. 2, element 68). Additionally, Roberts teaches the use of a decoder and latch circuit (24) which is used to control the scanning of the image sensor. More specifically, the decoder and latch circuit (24) includes a latch (104) for outputting a reset signal and latch (106) for outputting a row selection signal. See column 6, lines 30-45. Furthermore, Roberts discloses that the row selection and reset functions are implemented in a conventional row-by-row order. See column 7, lines 10-47. Thus, the examiner is interpreting the latch and decoder circuit (24) to be the row shift circuit which includes a row read scan circuit and a reset scan circuit. The Examiner acknowledges that the photoconverting element 42 in Fig. 2 of Roberts has an opposite orientation as the photoconverting element 20 in Fig. 10 of the instant application. The Examiner notes that while the polarity of the charge in the circuits of Fig. 2 of Roberts and Fig. 10 of the instant application

are opposite, the operation of the circuits are the same, i.e. the polarity of the charge is irrelevant to the function and effects of the circuits. It is noted that the Examiner has referenced both the first and second embodiments of Roberts. It is noted that the 2nd embodiment adds additional features to the 1st embodiment and includes all of the features of the 1st embodiment. See column 11, lines 50-68.

Roberts, however, fails to specifically disclose that the row shift circuit operates without a random access function. However, as per MPEP 2144.04(II)(A), the limitation of the row shift circuit "having no random access function" is considered a negative limitation. In effect, Roberts teaches a more complicated circuit which includes a random access function. The elimination of this feature from the circuit of Roberts would provide a row shift circuit that does not operate using a random access function. The elimination of this feature would further, result in a simplified row shift circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to eliminate the random access function of the row shift circuit of Roberts in order to simplify the circuit to a non-random access mode. See *In re Larson* 340 F.2d 965, 144 USPQ 347 (CCPA 1965) and *In re Kuhle*, 526 F.2d 553, 188 USPQ 7(CCPA 1975).

11. Regarding ***claim 4***, Roberts teaches a readout row-shifter (Fig. 4, element 102) for sequentially supplying the row selection signal to the row selection signal lines; a reset row-shifter (Fig. 4, element 100) for sequentially supplying the reset signal to the reset signal lines; and an image signal outputting device electrically connected to the output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal (col. 9, lines 1-7).

12. Regarding ***claim 5***, Roberts teaches at least one analog signal generator for converting the output signal generated on each output signal line (Fig. 9, CCVL) into an analog voltage signal (Fig. 6, Vout; col. 9, lines 1-17); and a row-directional shifter for controlling operation of the analog signal generator and for sequentially outputting the analog voltage signal from the at least one analog signal generator (col. 1, lines 15-20 and 62-65).

13. Regarding ***claim 6***, Roberts teaches an analog signal generator for converting the output signal generated on each output signal line into an analog voltage signal (col. 9, lines 1-17); and an analog-to-digital converter (Fig. 6, element 166) for receiving the analog voltage signal and for converting the analog voltage signal into a digital signal; and a buffer memory for receiving the digital signal, temporarily keeping the digital signal therein, and outputting the digital signal therefrom because a buffer is inherent in an A/D converter since the result is latched and held for a time in order to provide an output value.

14. Regarding ***claim 7***, Roberts teaches a controller (Fig. 1, element 208) for controlling operations (col. 13, lines 22-44) of the overall reset controller, the readout row-shifter, the reset row-shifter, and the image signal outputting device.

15. Regarding ***claim 8***, Roberts teaches a transfer signal line (Fig. 2, element 48) disposed for each pixel row; and a transfer control row-shifter for sequentially supplying (col. 5, line 6-13; col. 1, lines 62-65) a transfer control signal to the transfer signal lines, and each switching circuit further comprises a transfer transistor (Fig. 2, element 46) electrically connected between said cathode and gate of the photoelectric converter element and the gate of the output transistor, which gate is also connected to the reset transistor, the transfer transistor including a control terminal electrically connected to the transfer signal line.

16. Regarding ***claim 10***, Roberts discloses a readout row-shifter for sequentially supplying the row selection signal to said row selection signal lines (Fig. 3, element 114 row select); a reset row-shifter for sequentially supplying the reset signal to said reset signal lines (Fig. 3, element 112 row reset); and an image signal outputting device electrically connected to said output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal (Fig. 4, element 128, Fig. 6).

17. Regarding ***claim 11***, please see the rejection of claim 5.

18. Regarding ***claim 12***, please see the rejection of claim 6.

19. Regarding ***claim 13***, please see the rejection of claim 7.

20. C***laim 20*** is considered to be substantively equivalent to claim 1. Please see the discussion of claim 1 above.

21. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts (U.S. Pat. No. 5,452,004) in view of Ernest et al. (U.S. Pat. No. 4,827,348).

22. Regarding ***claim 14***, please see the rejections of claims 1 and 4. Furthermore, Roberts teaches the use of an additional transistor (Fig. 9, element 200) in an alternative embodiment that enables a global reset and "snap shot" capability (col. 12, lines 28-38). One of ordinary skill in the art would have provided the additional transistor of Roberts's alternative embodiment for the purpose of enabling still capture in addition to motion video capture. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided the additional transistor of Roberts's alternative embodiment for the purpose of enabling still capture in addition to motion video capture. Further still, Roberts teaches a still picture indication signal

generator for generating a still picture indication signal indicating shooting of a still picture (col. 12, lines 28-38) because a still picture indication signal is inherent in taking a snapshot.

Although Roberts teaches the use of an electronic shutter (col. 12, lines 46-50), Roberts does not disclose a light-shielding device capable of interrupting light incident to the image pickup device for a predetermined period of time after an overall reset operation. However, Ernest et al. teaches a mechanical shutter for interrupting light incident to an image pickup device (Fig. 3, element 24; col. 4, lines 11-15), which remains closed for a predetermined period of time until the still image is read out following an overall reset (Fig. 2). One of ordinary skill in the art would have provided the mechanical shutter of Ernest et al. for exposure control in a dual mode camera in order to permit high shutter speed in the still mode and electronic shuttering in the video mode (col. 3, lines 7-13). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the mechanical shutter of Ernest for exposure control in a dual mode camera in order to permit high shutter speed in the still mode and electronic shuttering in the video mode.

Furthermore, Ernest discloses a mobile picture mode controller (Fig. 3, element 20) electrically connected to said MOS-type solid-state image pickup device for continually controlling operation thereof for repeatedly conducting (a) an image readout operation in which the row selection signal is sequentially supplied from said readout row-shifter to a predetermined number of row selection signal lines for sequentially outputting from said image signal outputting device an image signal representing the output signal generated on each said output signal line (Fig. 3, Camera Timing and Control 20, CCD 12) because this is an inherent feature in a conventional CCD and (b) an electronic shutter operation (col. 2, lines 20-33) in which the

reset signal is sequentially supplied from said reset row-shifter to said reset signal supply line at least associated with said pixel row as an object of the image signal readout operation for sequentially discharge electric charge accumulated in said photoelectric converter elements (Fig. 3, Camera Timing and Control 20, CCD 12) because this is an inherent feature in a conventional CCD; and a first still picture mode controller (Fig. 3, element 20; Fig. 2, Still Switch On) electrically connected to said MOS-type solid-state image pickup device for controlling in place of said mobile mode controller, when the still picture indication signal is outputted, operations of said MOS-type solid-state image pickup device and said light shielding device, for conducting an overall reset operation in which the overall reset controller is operated, in a state in which the operations of said readout row-shifter and said rest row-shifter are stopped, and electric charge accumulated in all said photoelectric converter elements is discharged, and for conducting an image signal readout operation in which said light shielding device is operated and interrupts the incident light for a predetermined period of time after the overall reset operation is finished, and the row selection signal is sequentially supplied from said readout row-shifter to said row selection signal lines for sequentially outputting an image signal representing the output signal generated on said output signal lines from said image signal outputting device (Fig. 2, Still; col. 5, line 63-col. 6, line 48).

23. Regarding ***claim 15***, Ernest teaches when in the video mode (corresponding to an electronic shutter operation), and the still picture indication signal is outputted, the still picture mode controller does not interrupt the operation (Fig. 2, Still Switch On, Video, Still); when an electronic shutter operation is being executed at a point of time when the still picture indication signal is outputted, the still picture mode controller conducts once the image signal readout

operation once after the electronic shutter operation (Fig. 2, Still Switch On, Video, Still); and then the first still picture mode controller conducts the overall reset operation (col. 6, lines 28-59) when a global reset is operated in preparation for a second still picture.

24. Regarding ***claim 16***, please see the rejection of claim 8. Furthermore, Roberts teaches a mobile picture mode controller (Fig. 1, element 208) or the first still picture mode controller conducting the transfer control row-shifter for sequentially supplying, in the image readout operation, the row reset operation, or the overall reset operation, the transfer control signal to each transfer signal lines associated with the pixel row as an object of the operation.

25. **Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts (U.S. Pat. No. 5,452,004), in view of Ernest et al. (U.S. Pat. No. 4, 827, 348), and further in view of Soeda et al. (U.S. Pat. No. 5,382,974).**

26. Regarding ***claim 17***, Roberts teaches motion video and still image capture (col. 1, line 55-co1.2, line 5; col. 12, lines 28-38). Furthermore, Ernest teaches a shutter that interrupts light for a predetermined period of time (please see the rejection of claim 14). Neither Roberts nor Ernest teaches the use of a strobe device or a controller for a second still picture mode comprising a strobe device.

However, Soeda et al. teaches a strobe device (Fig. 1, element 20) for emitting flash light when a predetermined signal is received (Fig. 5) or the strobe device installing device for installing therein; a second still picture mode controller (strobe mode: col. 13, lines 27-31; Fig. 3, elements $8 and $18) electrically connected to the image pickup device for controlling in place of a mobile mode controller, when the still picture indication signal is outputted; a strobe

device operation signal is generated for operating the strobe device (Fig. 5); a shutter is operated for a predetermined period of time after strobe device operation signal is generated (Fig. 5); and a still picture mode specifying device (Fig. 3, element $8; col. 14, lines 24-38) for specifying a still picture mode controller to be operated when the still picture indication signal is outputted.

One of ordinary skill in the art would have provided the strobe of Soeda et al. with the imager of Roberts and Ernest et al. for the purpose of increasing the maximum photographable distance to an object and to obtain a high quality image (col. 13, line 65-col. 14, line 3). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the strobe of Soeda et al. with the imager of Roberts and Ernest et al. for the purpose of increasing the maximum photographable distance to an object and to obtain a high quality image (col. 13, line 65-col. 14, line 3).

27. Regarding ***claim 18***, Roberts teaches motion video and still image capture (col. 1, line 55-col. 2, line 5; col. 12, lines 28-38). Roberts does not specifically teach that a still picture mode does not interrupt a video mode when a still picture mode is indicated. However, Ernest et al. teaches an electronic shutter operation or an image signal readout operation is being executed at a point of time when the still picture indication signal is outputted, a still picture mode controller does not interrupt the operation; and when an electronic shutter operation is being executed at a point of time when the still picture indication signal is outputted, a still picture mode controller conducts the image signal readout operation once after the electronic shutter operation; and then a still picture mode controller conducts the overall reset operation (Fig. 2, Clear CCD; col. 5, line 63-co1.6, line 48).

28. Regarding ***claim 19***, please see the rejection for the rejection of claim 16.

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN M. VILLECCO whose telephone number is (571)272-7319. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOHN M. VILLECCO/
Primary Examiner, Art Unit 2622
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